

2 0 1 8

MATHEMATICS

(Special)

(Lower Grade Mathematics for Candidates with Special Learning Disabilities)

Full Marks : 100

Pass Marks : 30

Time : 3 hours

The figures in the margin indicate full marks for the questions

General Instructions :

- (i) All questions are compulsory.
- (ii) The question paper consists of 35 questions divided into four Sections A, B, C, and D.
- (iii) Section—A consists of 10 questions of 1 mark each.
Section—B is of 10 questions of 2 marks each.
Section—C is of 10 questions of 4 marks each.
Section—D is of 5 questions of 6 marks each.
- (iv) In Question Nos. 1 to 7 of Section—A there are four answers marked (A), (B), (C) and (D). Only one of these answers is correct. The letter indicating the correct answer should be written in capital in the answer book.
- (v) Use of Electronic device is not permitted.

Meghalaya Board Question Paper For Class 10

Maninder Kaur



Meghalaya Board Question Paper For Class 10:

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web apr 15 2021 i am trying to implement a 4 bit signed sequential multiplier i have a for loop in my tb but only the multiplicand changes not the multiplier when i manually change the multiplier i notice that my product outputs all 0s then it changes to the actual product what am i doing wrong

github rajat503 binary multiplier verilog code that multiplies a 4 - Nov 06 2022

web binary multiplier verilog code that multiplies a 4 bit binary input to a 3 bit binary input final project for digital design cs f215 uses shift and add technique

design of n bit binary multiplier using verilog hdl modelsim youtube - Jul 14 2023

web jun 7 2021 the speed of the multiplier is determined by both architecture and circuit this design presents the design and implementation of n bit binary multiplier logic we used modelsim software

verilog 8 bit sequential multiplier using add and shift stack overflow - Oct 05 2022

web aug 30 2020 i m designing an 8 bit signed sequential multiplier using verilog the inputs are clk clock rst reset a 8 bit multiplier b 8 bit multiplicand and the outputs are p product and rdy ready signal indicating multiplication is over

lab 1 sequential multiplier nctu - Dec 07 2022

web you cannot use the multiplication operator of verilog the lab file submission deadline is on 9 28 by 6 00pm write simulation for a multiplier the input output ports of the 8 bit multiplier is as follows module seqmultiplier input wire clk input wire enable input wire 7 0 a input wire 7 0 b output wire 15 0 c